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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/603,041 | 06/24/2003 | Steven Alan Lytle | Lytle 22-15-20 | 2383 |

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Docket Administrator Agere Systems Inc.
Room 4u533C
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Berkeley Heights, NJ 07922-2747

| EXAMINER | |
|---|---|
| GHYKA, ALEXANDER G | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/603,041 | LYTLE ET AL. | |
| | Examiner | Art Unit | |
| | Alexander G. Ghyka | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

ALEXANDER GHYKA
PRIMARY EXAMINER
AU 2812

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicants' response of 4/12/2006 has been considered and entered in the record. Claim 12 has been cancelled. Claims 1-11 and 13-17 are now under consideration. Applicant's arguments have been considered but they are not persuasive for the reasons as discussed below.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1-9 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian (US 6,060,380) in view of Kudoh et al (EP 0 394 722).**

The present Claims generally call for a process for manufacturing an integrated circuit comprising providing a substrate comprising a dielectric layer over a conductive material; depositing a hardmask; applying a first photoresist over the hardmask and photodefining at least one first elongated opening; etching the hardmask and partially etching the dielectric to deepen the at least one first elongated opening to form a trench the trench having a bottom in the dielectric layer *with no etch stop layer formed thereon*; removing the first photoresist; applying a second photoresist and photodefining at least one second elongated opening transverse to the at least one trench so as to expose a portion of the dielectric defined by an intersection of the first and second openings; and etching the exposed dielectric from the bottom of the at least one trench down to the underlying conductive material.

Subramanian et al disclose a process for manufacturing interconnection structures in an integrated circuit comprising providing a substrate comprising a dielectric layer over a conductive material; depositing a hardmask; applying a first photoresist over the hardmask and photodefining at least one first elongated opening; etching the hardmask and partially etching the dielectric to deepen the at least one first elongated opening to form a trench, the trench having a bottom in the dielectric layer; removing the first photoresist; applying a second photoresist and photodefining at least

a second opening across the trench and etching the exposed dielectric from the bottom of the at least one trench down to the underlying conductive material. See column 5, line 25 to column 6, line 15. Moreover, Subramanian disclose that the hardmask can be silicon nitride as required by present Claim 6. See column 4, lines 65-68. Subramanian also disclose metallization and planarization as required by present Claim 4. See column 6, lines 8-20. Furthermore, Subramanian disclose a square cross section as required in Claims 8 and 9. See Figure 2. Furthermore, Subramanian et al illustrates forming " a trench the trench having a bottom in the dielectric layer with no etch sop layer formed thereon", as required by the present Claims. See Figure 4G and column 4, lines 40-68. There is no etch stop layer formed at the bottom of the trench as the trench is etched all the way down to the conductor level.

Subramanian et al differs from the present Claims in that it does not disclose that the second opening is elongated, and transverse and perpendicular to the trench.

Kudoh el al disclose the formation of interconnect structures which comprises forming a via at the intersection of a trench and an elongated opening in the photoresist which is traverse and perpendicular to the trench. See column 5, lines 20-50 and Figures 3, 4, 5A-E and 6. Kudoh et al discloses that this method reduces wiring pitch in the interconnect structure. See column 2, lines 50-56.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to form a via at the intersection of a trench and an elongated opening in the photoresist which is traverse and perpendicular to the trench as disclosed by Kudoh et al, in the process of forming interconnects as disclosed by Subramanian et al, for its

known benefit in the art in reducing wiring pitch in interconnects as disclosed by Kudoh et al. As both references are drawn to processes of making interconnects, a *prima facie* case of obviousness is established.

**Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian (US 6,060,380) in view of Kudoh et al (EP 0 394 722) as applied to claims 1-9 and 13-17 above, and further in view of Yang et al (US 6,162,587).**

Subramanian (US 6,060,380) and Kudoh et al (EP 0 394 722) are relied upon as discussed above.

However, Subramanian (US 6,060,380) and Kudoh et al (EP 0 394 722) do not disclose a connection having a rectangular cross section having a feature size of 0.5 microns or less.

Yang et al disclose (column 5, line 50 to column 6, line 5) an integrated circuit comprising at least one connection, the connection having a quadrilateral cross section and a feature size of 0.5 microns or less.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to form a rectangular cross section having a feature size of 0.5 microns or less using the process of Subramanian et al and Kudoh et al, as Yang et al disclose the equivalence of square and rectangular connects, and the fact that connects of 0.5 microns or less are known in the art. In light of the disclosure of Yang et al that both square and rectangular connects are known in the art, it would have been obvious for one of ordinary skill in the art to use the process of Subramanian et al and Kudoh et al

to produce a rectangular connect, for its known benefit in the art as a connect. Moreover, as Yang et al disclose the formation of connects of 0.5 microns or less, the formation of such a connect with the process of Subramanian et al and Kudoh et al, would simply be a matter of optimization. Discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. See *In re Antonie*, 195 USPQ 6 (CCPA 1977). Therefore, a *prima facie* case of obviousness is established.

***Response to Applicants' Arguments***

Applicants argue that the independent Claims have been amended to include the limitation that no etch stop layer is used at the bottom of the trench, and thus the claims are distinguishable over the cited prior art. Applicants argue that a high dielectric layer such as SiN is avoided during the claimed process and Subramanian et al employs a hard mask layer as an etch stop before etching down to the conductor 102. The Examiner maintains that as Subramanian discloses etching all the way down to the conductor level there is no "etch stop layer formed" at the bottom of the trench. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no etch stop layer used) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The present Claims as written simply require that "no etch stop layer is formed" on the

bottom of the trench. In the Subramanian reference there is no etch stop layer formed on the bottom of the trench, as the trench goes all the way down to the conductor level as shown in Figure 4G. Therefore the present Claims are not distinguishable over the cited prior art.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Friday during general business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGG
June 21, 2006

ALEXANDER GHYKA
PRIMARY EXAMINER

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